

I2S bus with buffer IC Timing Test Report

Project code	HW Version	SW Version	
K18X001T00	V115	19.522.43 (2021.02.01)	
Tester	Tom lee	Test date	2021/03/16

1.1 Test Steps

1.1.1 Connect main board and sub-board as environment

1.1.2 Power on DUT

1.1.3 Connect J806 (AUX IN) to mobile phone, then plays YouTube video.

1.1.4 When speaker have music, then start to measure I2S wave.

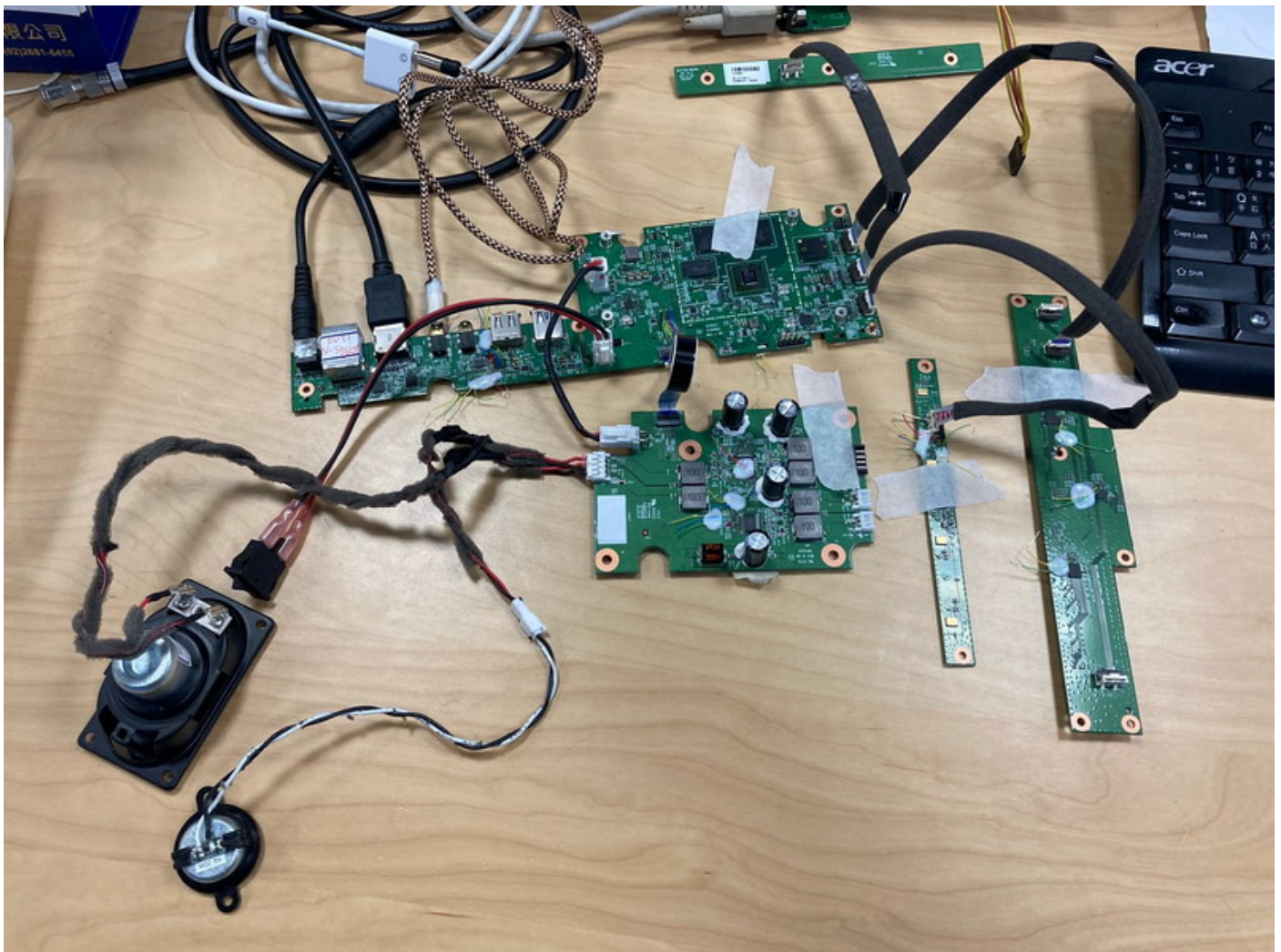
1.1.5 Measurement point.

AD82584F: BCLK: R2808, LRCK: R2810, Data: R2811

AD83586B: BCLK: R2833, LRCK: R2834, Data: R2835

ADC3100: BCLK: R2946, LRCK: R2947, Data: R2948

CX20810: BCLK: R6_17, LRCK: R6_19, Data: R6_18

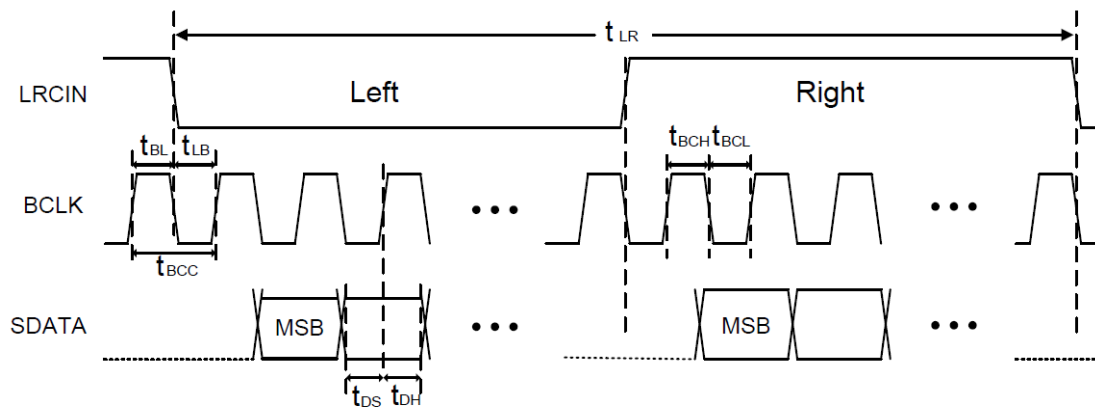


Environment Picture

1.2 Specification

1.2.1 Class-D AMP AD82584F

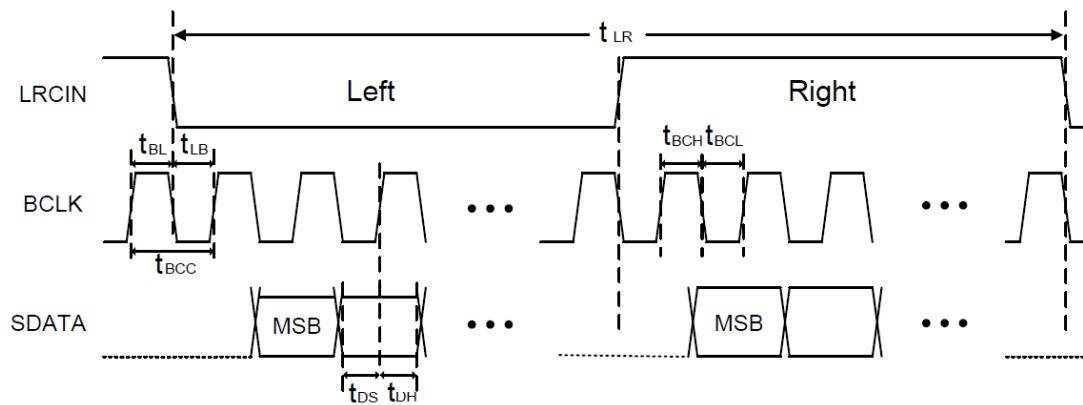
- Timing Relationship (Using I²S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	5.2		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	25			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	25			ns
t_{BCC}	BCLK Period ($1/64F_S$)	81.38		488.3	ns
t_{BCH}	BCLK Pulse Width High	40.69		244	ns
t_{BCL}	BCLK Pulse Width Low	40.69		244	ns
t_{DS}	SDATA Set-Up Time	25			ns
t_{DH}	SDATA Hold Time	25			ns

1.2.2 Class-D AMP AD83586B

- Timing Relationship (Using I²S format as an example)



Symbol	Parameter	Min	Typ	Max	Units
t_{LR}	LRCIN Period ($1/F_S$)	10.41		31.25	μs
t_{BL}	BCLK Rising Edge to LRCIN Edge	50			ns
t_{LB}	LRCIN Edge to BCLK Rising Edge	50			ns
t_{BCC}	BCLK Period ($1/64F_S$)	162.76		488.3	ns
t_{BCH}	BCLK Pulse Width High	81.38		244	ns
t_{BCL}	BCLK Pulse Width Low	81.38		244	ns
t_{DS}	SDATA Set-Up Time	50			ns
t_{DH}	SDATA Hold Time	50			ns

1.2.3 Audio ADC TLV320ADC3100

7.8 Timing Requirements: I²S, LJF, RJF Timing in Slave Mode

specified at 25°C, DVDD = 1.8 V, all timing specifications are measured at characterization; see Figure 3 for a timing diagram

		IOVDD = 1.8 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t _H (BCLK)	BCLK high period	35		35		ns
t _L (BCLK)	BCLK low period	35		35		ns
t _S (WS)	BCLK, WCLK setup time	10		6		ns
t _H (WS)	BCLK, WCLK hold time	10		6		ns
t _d (DO-WS)	BCLK, WCLK to DOUT delay time (for LJF mode only)		30		30	ns
t _d (DO-BCLK)	BCLK to DOUT delay time		25		20	ns
t _r	Rise time		16		8	ns
t _f	Fall time		16		8	ns

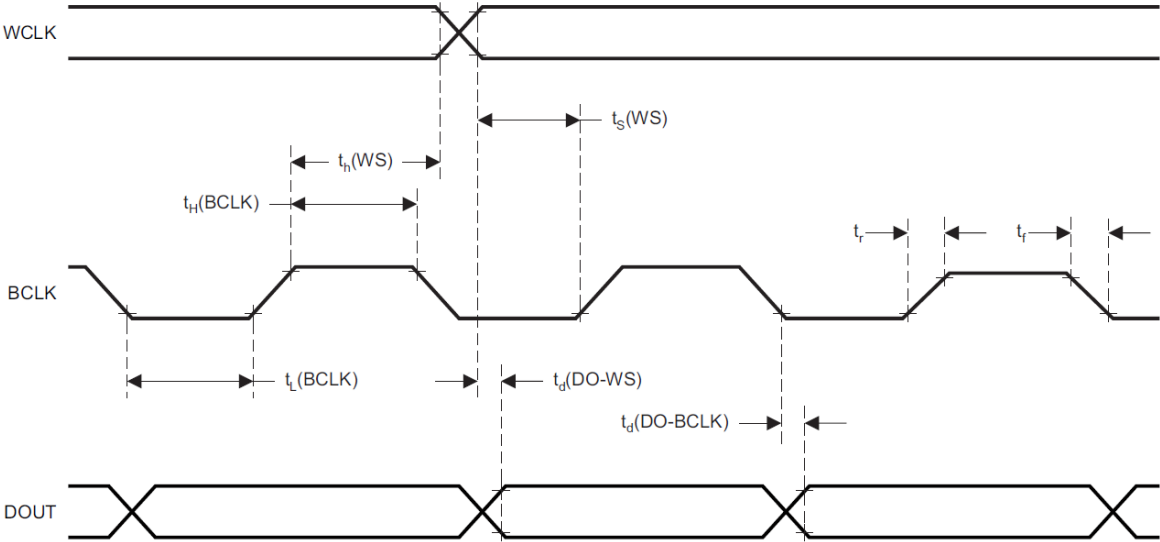


Figure 3. I²S, LJF, RJF Timing in Slave Mode

1.2.4 ADC CX20810

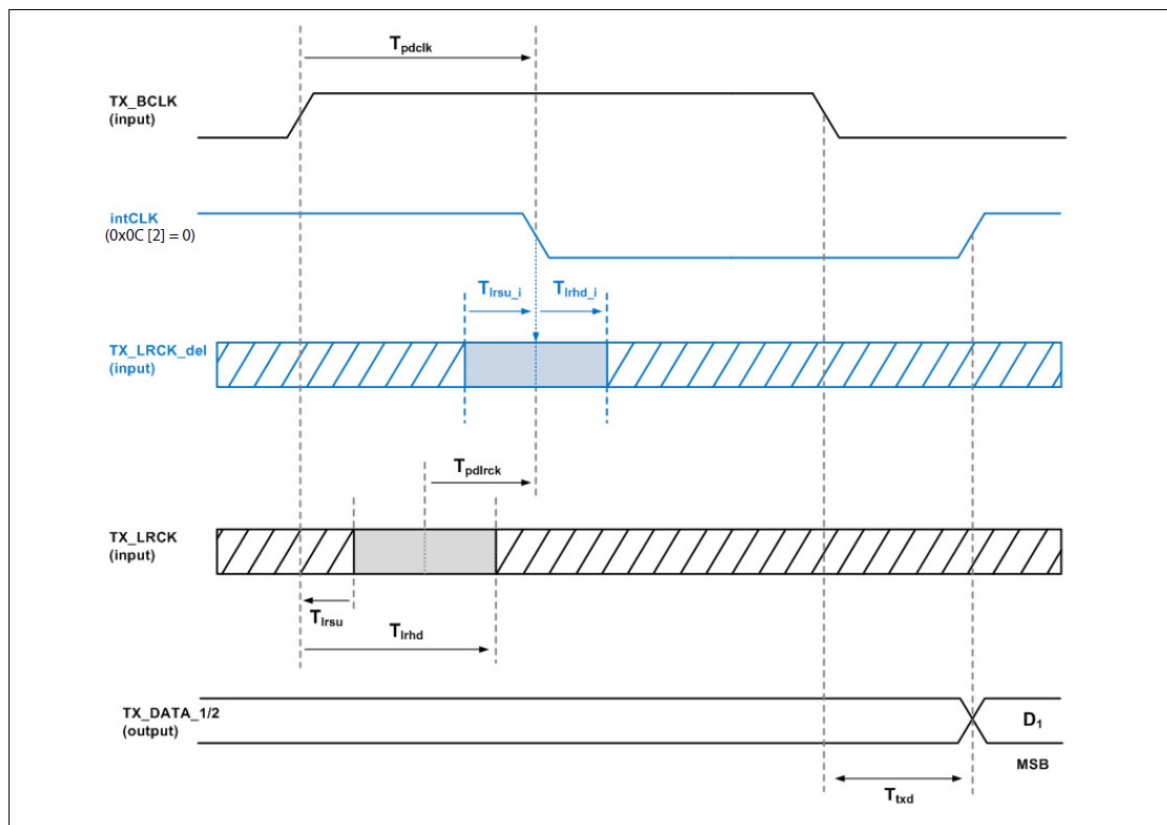


Figure 85: Slave Mode Timing Diagram: Data Transitions on Falling Edge of BCLK

- The BCLK and LRCK signals experience internal propagation delays due to pad and logic delays
- The internal logic setup and hold time requirements are less than 50 ps and are negligible relative to the propagation delay.
- Based on the worst case values, the minimum required setup time is -5 ns and minimum hold time is 7 ns. This is relative to the LRCK and BCLK signals seen at the device pins.
- Proper interface configuration will ensure around a half-cycle (~40 ns) of timing margin.

Table 114: Slave Mode Timing Specification

Parameter	Symbol	Min	Typ	Max	Unit
I2S/TDM bit clock cycle time	T_{CC}	80	81.38	–	ns
Internal propagation delay for TX_BCLK	T_{PDCLK}	10	–	12	ns
Internal propagation delay for TX_LRCK	T_{PDLRCK}	5	–	7	ns
TX_LRCK to TX_BCLK setup time	T_{LRSU}	-5	–	–	ns
TX_LRCK to TX_BCLK hold time	T_{LRHD}	+7	–	–	ns
TX Data propagation delay from falling edge of BCLK	T_{TXD}	5	–	20 *	ns

* Output delay assumes 3.3V IO and 30 pF load. For 1.8v IO and 20 pF load the max delay is 32 ns

1.3 Test Result

Chip	Parameter	Symbol	Min	Max	Unit	Result	Pass /Fail	Figure
AD 82584F	LRCIN Period (1/FS)	tLR	5.2	31.25	us	20.836	Pass	1
	BCLK Rising Edge to LRCIN Edge	tBL	25		ns	165.51	Pass	2
	LRCIN Edge to BCLK Rising Edge	tLB	25		ns	159.77	Pass	3
	BCLK Period (1/64FS)	tBCC	81.38	488.3	ns	325.61	Pass	4
	BCLK Pulse Width High	tBCH	40.69	244	ns	159.99	Pass	5
	BCLK Pulse Width Low	tBCL	40.69	244	ns	161.14	Pass	6
	SDATA Set-Up Time	tDS	25		ns	159.59	Pass	7
	SDATA Hold Time	tDH	25		ns	167.34	Pass	8
AD 83586B	LRCIN Period (1/FS)	tLR	5.2	31.25	us	20.837	Pass	9
	BCLK Rising Edge to LRCIN Edge	tBL	25		ns	165.50	Pass	10
	LRCIN Edge to BCLK Rising Edge	tLB	25		ns	159.43	Pass	11
	BCLK Period (1/64FS)	tBCC	81.38	488.3	ns	324.77	Pass	12
	BCLK Pulse Width High	tBCH	40.69	244	ns	159.72	Pass	13
	BCLK Pulse Width Low	tBCL	40.69	244	ns	159.43	Pass	14
	SDATA Set-Up Time	tDS	25		ns	159.99	Pass	15
	SDATA Hold Time	tDH	25		ns	166.37	Pass	16
TLV320 ADC3100	BCLK high period	tH(BCLK)	35		ns	162.37	Pass	17
	BCLK low period	tL(BCLK)	35		ns	162.16	Pass	18
	BCLK, WCLK setup time	ts(WS)	6		ns	157.22	Pass	19
	BCLK, WCLK hold time	th(WS)	6		ns	167.43	Pass	20
	BCLK to DOUT delay time	td(DO-BCLK)		20	ns	9.017	Pass	21
	Rise time	tr		8	ns	0.517	Pass	22
	Fall time	tf		8	ns	0.855	Pass	23
CX20810	TX_LRCK to TX_BCLK setup time	TLRSU	-5	-	ns	170.68	Pass	24
	TX_LRCK to TX_BCLK hold time	TLRHD	+7	-	ns	154.77	Pass	25
	TX Data propagation delay from falling edge of BCLK	TTXD	5	20	ns	13.258	Pass	26

1.4 Wave

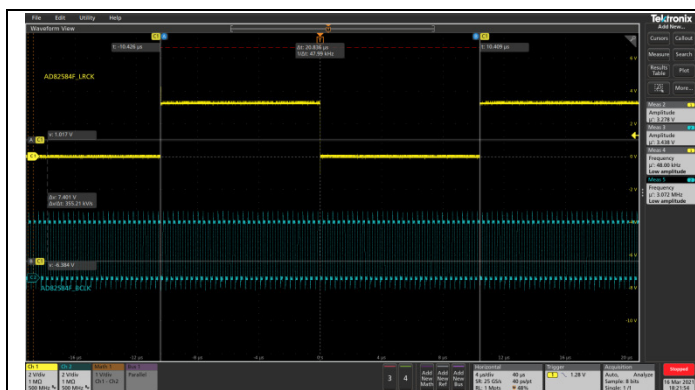


Figure 1: LRCIN Period (1/FS)

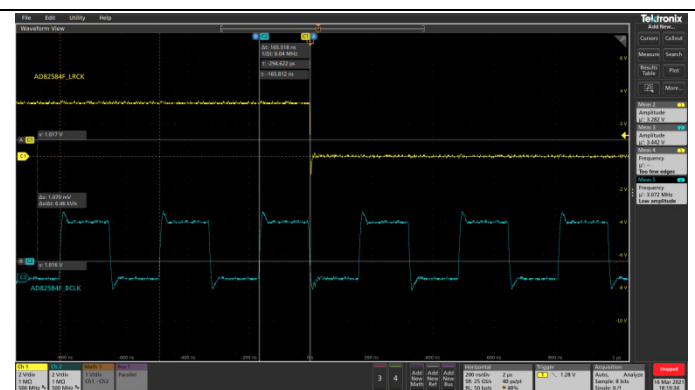


Figure 2: BCLK Rising Edge to LRCIN Edge

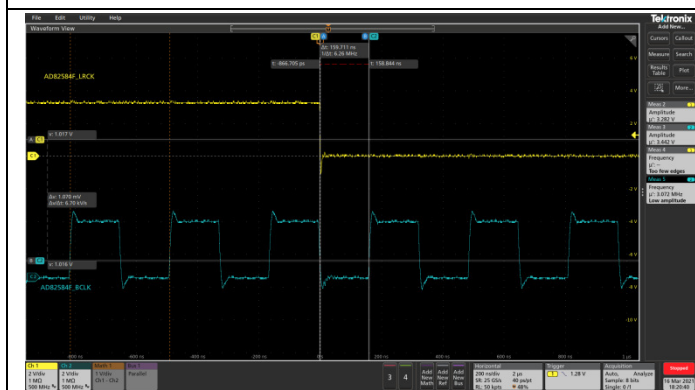


Figure 3: LRCIN Edge to BCLK Rising Edge

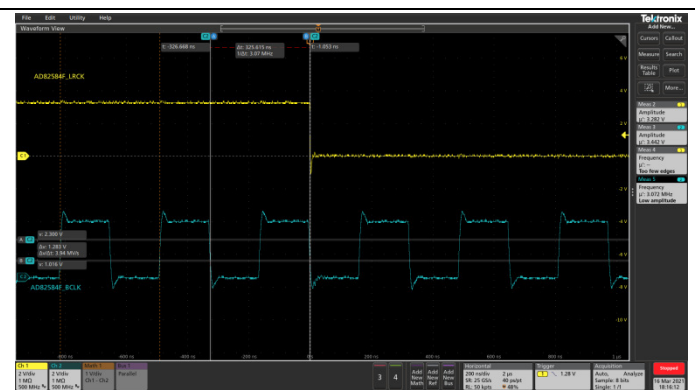


Figure 4: BCLK Period (1/64FS)

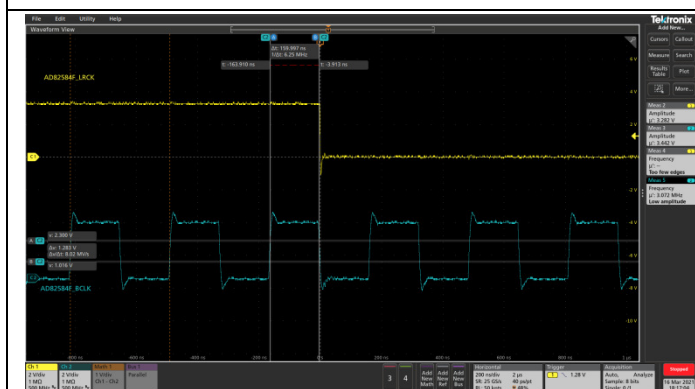


Figure 5: BCLK Pulse Width High

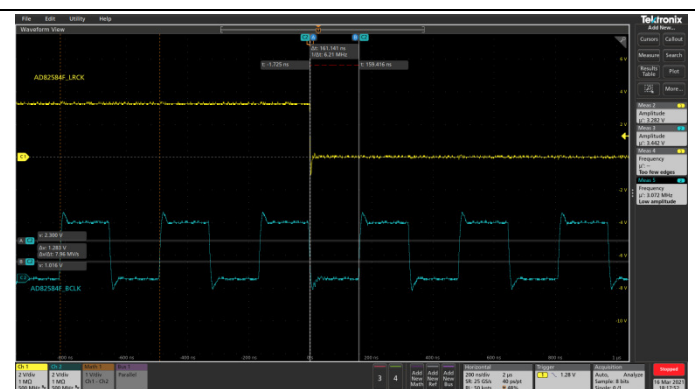


Figure 6: BCLK Pulse Width Low

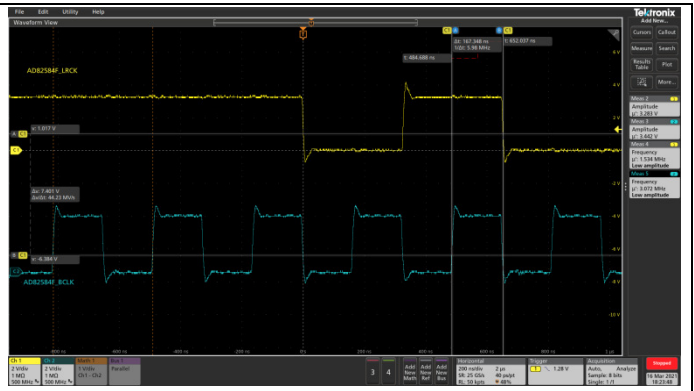
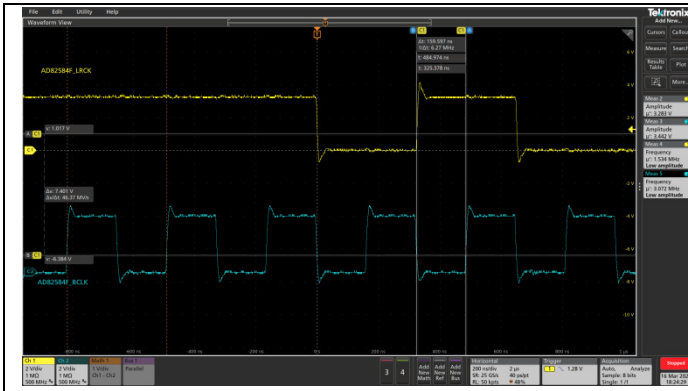


Figure 7: SDATA Set-Up Time

Figure 8: SDATA Hold Time

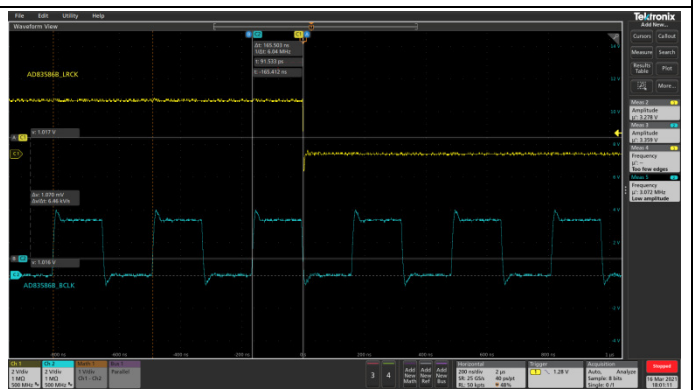
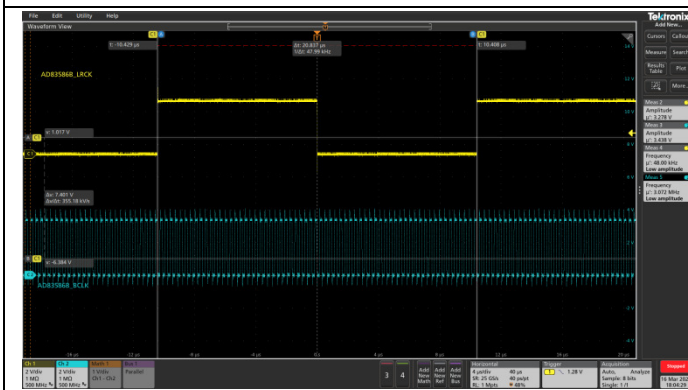


Figure 9: LRCIN Period (1/FS)

Figure 10: BCLK Rising Edge to LRCIN Edge

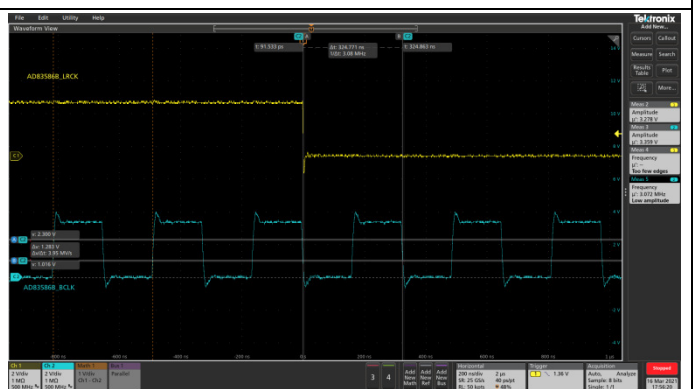
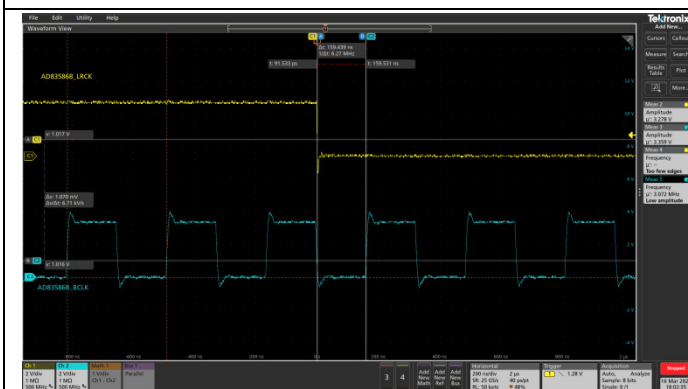


Figure 11: LRCIN Edge to BCLK Rising Edge

Figure 12: BCLK Period (1/64FS)

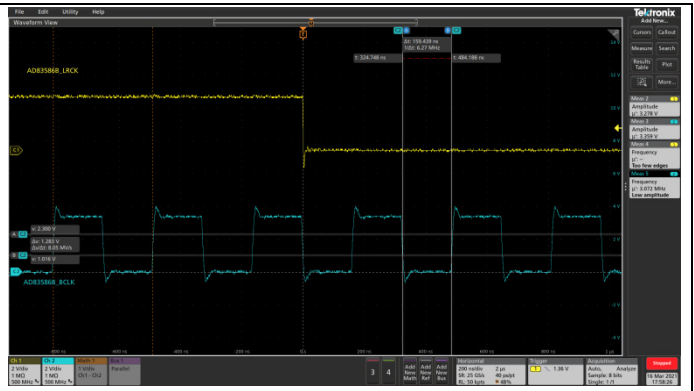
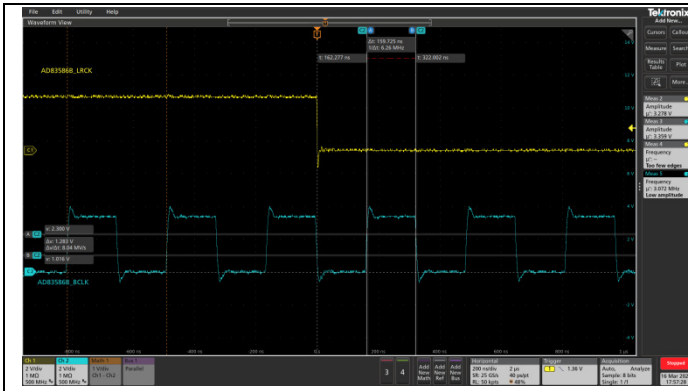


Figure 13: BCLK Pulse Width High

Figure 14: BCLK Pulse Width Low

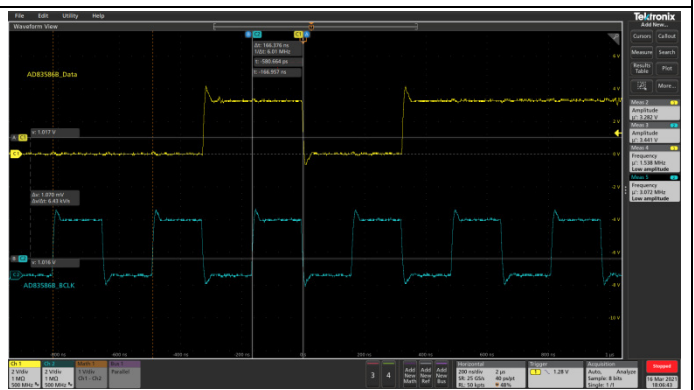
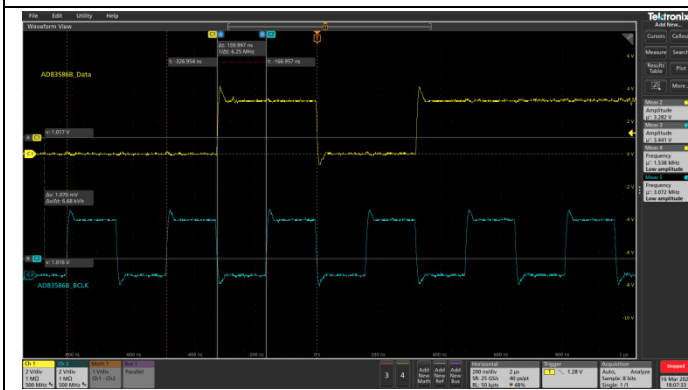


Figure 15: SDATA Set-Up Time

Figure 16: SDATA Hold Time

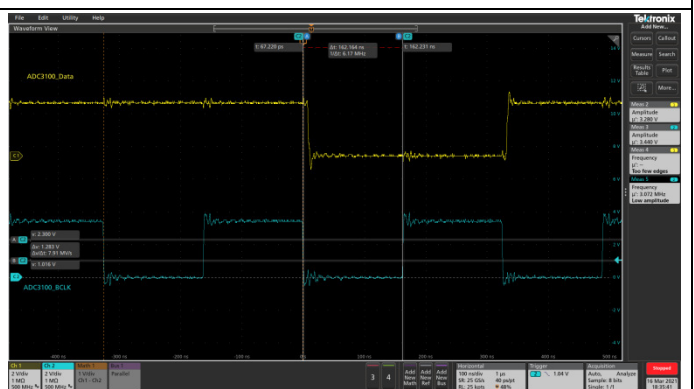
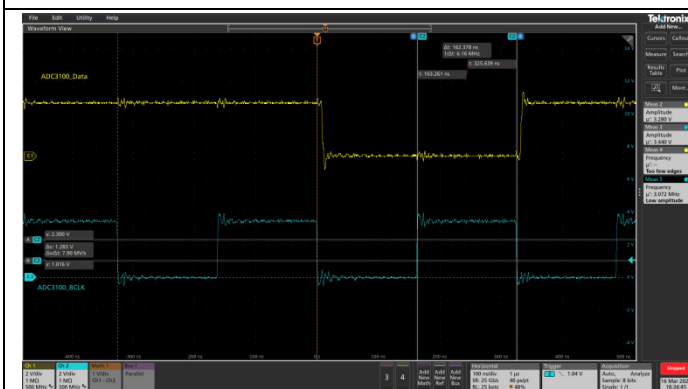


Figure 17: BCLK high period

Figure 18: BCLK low period

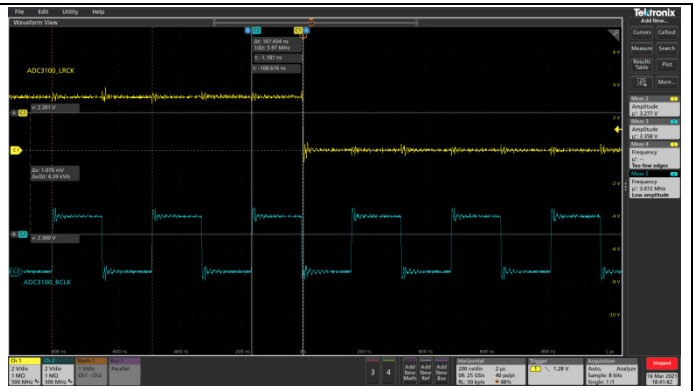
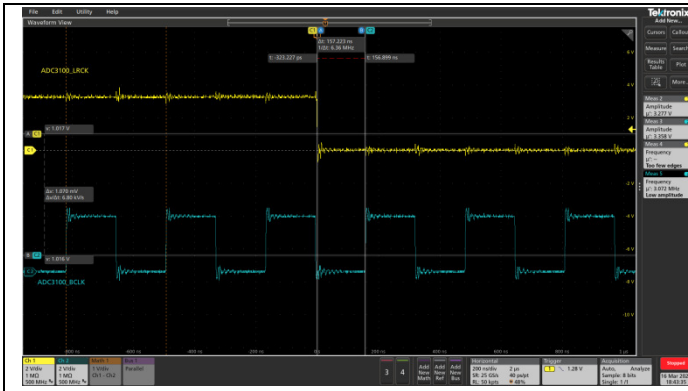


Figure 19: BCLK, WCLK setup time

Figure 20: BCLK, WCLK hold time

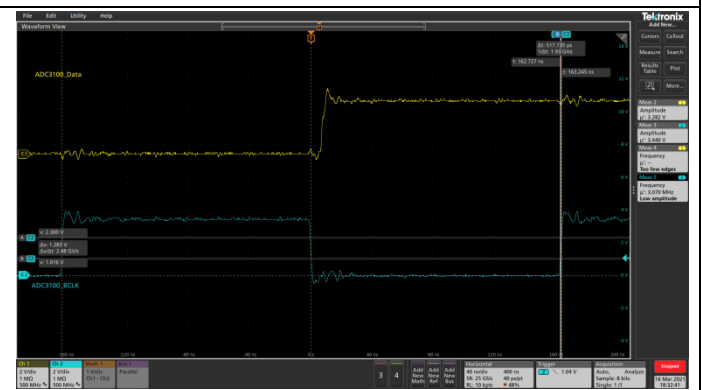
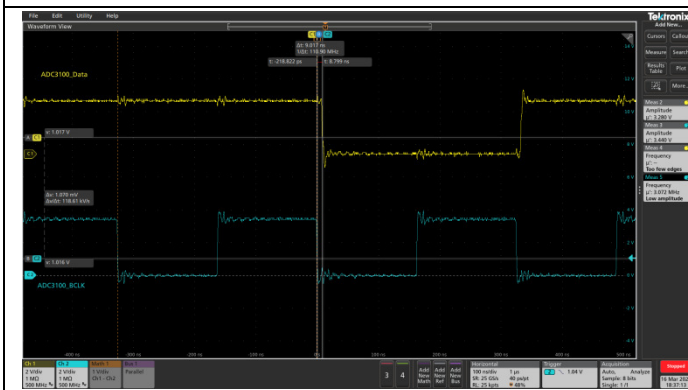


Figure 21: BCLK to DOUT delay time

Figure 22: Rise time

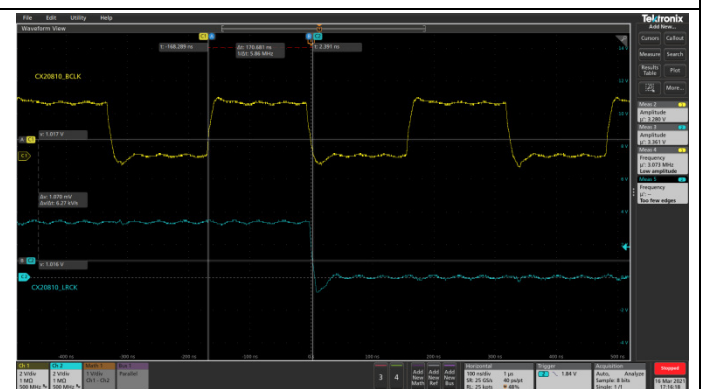
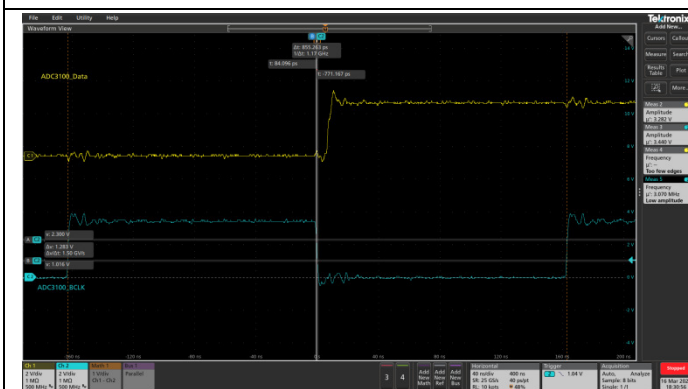


Figure 23: Fall time

Figure 24: TX_LRCK to TX_BCLK setup time

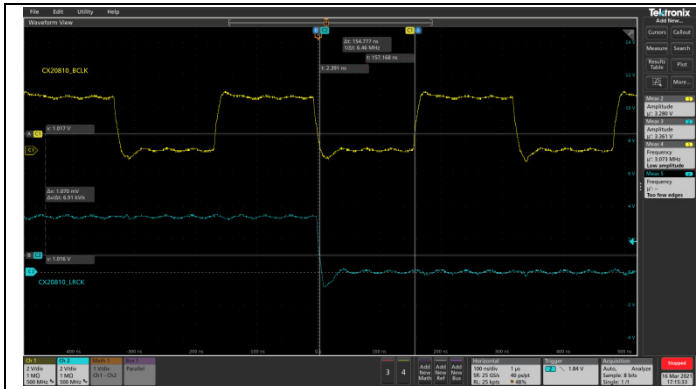


Figure 25: TX_LRCK to TX_BCLK hold time

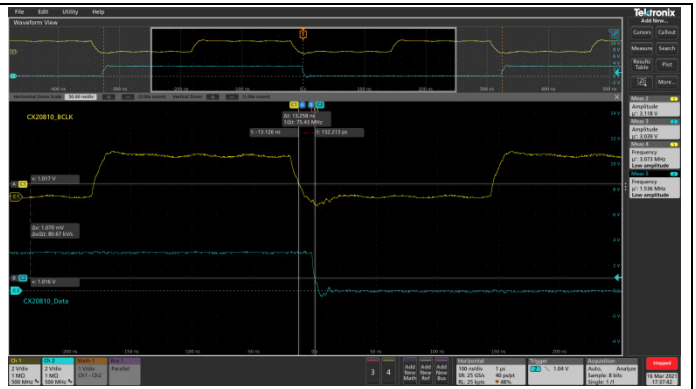


Figure 26: TX Data propagation delay from falling edge of BCLK